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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,552	09/15/2003	John Joseph Konrad	END920000077US2	9045

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EXAMINER

PATEL, ISHWARBHAI B

ART UNIT PAPER NUMBER

2841

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/661,552

**Applicant(s)**

KONRAD ET AL.

**Examiner**

Ishwar (I. B.) Patel

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 June 2004.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 32-41 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 32-41 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 15 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election of specie I, group II, an electronic structure, claims 32-41, in the reply filed on June 24, 2004, is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 32, 34 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Echigo et al., US Patent No. 6,274,821.

**Regarding claim 32**, Echigo et al., discloses an electronic structure having embedded substantially flush circuit features comprising:

a rigid first dielectric layer (1, figure 1) of a first polymeric material (glass-epoxy substrate, column 3, line 13-14) having a substantially flush first major surface (see figure 1); a circuitry layer (L3i, figure 1) having a substantially flush second major surface formed on said first major surface and a substantially flush

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third major surface substantially parallel to said second surface; and a second dielectric layer (L3R, figure 1) of a second dielectric polymer having a substantially flush fourth major surface formed on said third surface.

**Regarding claim 34**, Echigo et al., further discloses the first dielectric layer comprises glass as reinforcing material, as applied to claim 32 above.

**Regarding claim 35**, Echigo et al., further discloses the dielectric polymers selected from thermosetting resins (Echigo et al, column 3, line 57-67).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 33, 37, 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Echigo et al., as applied to claims 32, 34 and 35 above, and further in view of Strandberg et al., US Patent No. 6,323,435.

**Regarding claim 33**, Echigo et al., discloses the circuitry layer comprising a layer of third dielectric polymer (L3ia, figure 1), but fails to explicitly disclose the

conductive features formed with a seed layer having conductive layer plated on seed layer.

However, as disclosed by Strandberg et al., seed layer for forming the conductive patterns on a dielectric material is well known in the art. Strandberg et al., discloses a copper seed layer of approximately 2,000 angstroms thick, and further discloses that in a preferred embodiment the seed layer of a chrome/copper stack where the chrome layer is an adhesive layer approximately 200 angstroms thick, and the overlying copper layer is approximately 2000 angstroms thick, column 8, line 36-44.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the board of Echigo et al., with the circuit features formed by providing a seed layer and forming the conductive layer on the seed layer, as taught by Strandberg and as is well known in the art.

The sidewall for the circuit features made by laser ablation is process limitation in the product claim. Such a process limitation defines the claimed invention over the prior art only to the degree it defines the product itself. A process limitation cannot serve to patentably distinguish the product over prior art, in the case that the product is the same as, or obvious over, the prior art. See *Product-by-Process* in MPEP 2113 and 2173.05(p) and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985).

**Regarding claim 37**, Echigo et al. and Strandberg, further discloses the conductive material of the circuit features comprises copper (Echigo et al, column 3, line 33-37).

**Regarding claim 40**, the combination of Echigo et al. and Strandberg, further discloses the seed layer comprises copper as applied to claim 33 above.

**Regarding claim 41**, the combination of Echigo et al. and Strandberg, further discloses the seed layer is approximately 2,000 angstroms thick, as applied to claim 33 above, which is within the claimed range of 100 to 5000 angstroms.

6. Claims 36, 38 and 39 rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Echigo et al., as applied to claims 32, 34 and 35 above, and further in view of Strandberg et al., US Patent No. 6,586,682.

**Regarding claim 36, 38 and 39**, the applicant is further claiming the circuitry layer up to about 20 micron thick, as claimed in claim 36, about 5 to about 20 microns thick as claimed in claim 38 and about 5 to about 10 microns thick as claimed in claim 39.

Echigo et al. is silent about the thickness of the circuitry feature.

Strandberg et al., discloses printed circuit board with thin film technology to create a high density interconnect structure, column 1, line 5-10 and further disclose pattern metal layer and dielectric layer having thickness less than or equal to about 10 microns (figure 4, column 7, line 10-26).

A person of ordinary skill in the art would have recognized the advantage of providing thin circuitry layers to increase the interconnect density.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the combination structure of Yoneda and Echigo et al., with the circuitry layer with a thickness of up to about 20 micron thick, as claimed in claim 36, about 5 to about 20 microns thick as claimed in claim 38 and about 5 to about 10 microns thick as claimed in claim 39, as taught by Strandberg, in order to increase the interconnect density.

### ***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Norman Davey	US Patent No. 3,622,384.
Isawa et al.,	US Patent No. 4,970,354.
Lake et al.,	US Patent No. 4,915,983.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

I B Patel  
Examiner  
Art Unit: 2841  
September 10, 2004



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